CLAIMS

What is claimed is:

1. An encoder that performs both LDPC (Low Density Parity Check) encoding and modulation encoding on a binary sequence to generate an LDPC coded modulation signal, the encoder comprising:

an LDPC encoder that performs LDPC coding on the binary sequence to generate an LDPC codeword that includes a plurality of LDPC coded bits;

an S/P (Serial to Parallel) mapping functional block that divides the LDPC codeword into a plurality of paths such that each path of the plurality of paths outputs selected LDPC coded bits of the plurality of LDPC coded bits;

wherein LDPC coded bits that are output from the plurality of paths are grouped together to form a plurality of LDPC coded symbols;

a plurality of modulation encoders operating cooperatively such that each modulation encoder of the plurality of modulation encoders selectively receives certain LDPC coded symbols of the plurality of LDPC coded symbols according to a predetermined cycle;

wherein each modulation encoder of the plurality of modulation encoders performs modulation encoding on the LDPC coded symbols of the plurality of LDPC coded symbols that it receives thereby generating corresponding pluralities of LDPC coded modulation symbols; and

wherein LDPC coded modulation symbols are selected from the corresponding pluralities of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

2. The encoder of claim 1, wherein:

the S/P mapping functional block divides the LDPC codeword into 3 paths;

a second n bits of the plurality of LDPC coded bits of the LDPC codeword are provided to a first path of the 3 paths;

a last n bits of the plurality of LDPC coded bits of the LDPC codeword are provided to a second path of the 3 paths; and

a first n bits of the plurality of LDPC coded bits of the LDPC codeword are provided to a third path of the 3 paths.

3. The encoder of claim 1, wherein:

the S/P mapping functional block divides the LDPC codeword into 3 paths;

a first bit is selected from a first path of the 3 paths;

a second bit is selected from a second path of the 3 paths;

a third bit is selected from a third path of the 3 paths; and

the first bit, the second bit, and the third bit form are grouped together to form a 3 bit LDPC coded symbol.

4. The encoder of claim 1, wherein:

the plurality of modulation encoders includes a first modulation encoder and a second modulation encoder;

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

the first modulation encoder receives all of the LDPC coded symbols of the first plurality of LDPC coded symbols and odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols; and

the second modulation encoder receives even numbered LDPC coded symbols of the second plurality of LDPC coded symbols.

5. The encoder of claim 1, wherein:

the plurality of modulation encoders includes a first modulation encoder, a second modulation encoder, and a third modulation encoder;

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

the first modulation encoder receives all of the LDPC coded symbols of the first plurality of LDPC coded symbols;

the second modulation encoder receives even numbered LDPC coded symbols of the second plurality of LDPC coded symbols; and

the third modulation encoder receives odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols.

6. The encoder of claim 1, wherein:

the plurality of modulation encoders includes a first 8 PSK (8 Phase Shift Key) modulation encoder and a second 8 PSK modulation encoder;

the first 8 PSK modulation encoder performs modulation encoding using a first modulation on the LDPC coded symbols that it receives thereby generating a first corresponding plurality of LDPC coded modulation symbols;

the second 8 PSK modulation encoder performs modulation encoding using a second modulation on the LDPC coded symbols that it receives thereby generating a second corresponding plurality of LDPC coded modulation symbols; and

LDPC coded modulation symbols are selected from the first corresponding plurality of LDPC coded modulation symbols and the second corresponding plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

7. The encoder of claim 1, wherein:

the plurality of modulation encoders includes a first 8 PSK (8 Phase Shift Key) modulation encoder, a second 8 PSK modulation encoder, and a third 8 PSK modulation encoder;

the first 8 PSK modulation encoder performs modulation encoding using a first modulation on the LDPC coded symbols that it receives thereby generating a first corresponding plurality of LDPC coded modulation symbols;

the second 8 PSK modulation encoder performs modulation encoding using a second modulation on the LDPC coded symbols that it receives thereby generating a second corresponding plurality of LDPC coded modulation symbols;

the third 8 PSK modulation encoder performs modulation encoding using a third modulation on the LDPC coded symbols that it receives thereby generating a third corresponding plurality of LDPC coded modulation symbols; and

LDPC coded modulation symbols are selected from the first corresponding plurality of LDPC coded modulation symbols, the second corresponding plurality of LDPC coded modulation symbols, and the third corresponding plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

8. The encoder of claim 1, wherein:

each modulation encoder of the plurality of modulation encoders performs modulation encoding on the LDPC coded symbols of the plurality of LDPC coded symbols that it receives according to a modulation corresponding to that modulation encoder;

each modulation encoder employs a modulation that is different that the modulations employed by the other modulation encoders when performing modulation encoding that is different that the modulation employed by the other modulation encoders; and

each modulation includes a constellation and a corresponding mapping.

9. The encoder of claim 1, wherein:

the LDPC variable modulation signal includes a plurality of LDPC coded modulation symbols;

a first LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a second modulation that includes a second constellation and a corresponding second mapping.

10. The encoder of claim 9, wherein:

the first constellation and the second constellation are both 8 PSK (8 Phase Shift Key) shaped constellations;

the first modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the corresponding first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the corresponding second mapping.

11. The encoder of claim 1, wherein:

the LDPC encoder performs variable code rate LDPC coding on the binary sequence to generate the LDPC codeword such that the LDPC codeword is a variable code rate LDPC codeword;

the S/P mapping functional block that divides the variable code rate LDPC codeword into the plurality of paths such that each path of the plurality of paths outputs selected LDPC coded bits of the plurality of LDPC coded bits;

the LDPC coded bits that are output from the plurality of paths are grouped together to form a plurality of LDPC coded symbols such that a first LDPC coded symbol includes a first number of bits and a second LDPC coded symbol includes a second number of bits; and

the formed LDPC coded modulation signal that is an LDPC variable modulation signal is also an LDPC variable code rate signal.

12. The encoder of claim 1, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

13. An encoder that performs both LDPC (Low Density Parity Check) encoding and modulation encoding on a binary sequence to generate an LDPC coded modulation signal, the encoder comprising:

an LDPC encoder that performs variable code rate LDPC coding on the binary sequence to generate a variable code rate LDPC codeword that includes a plurality of LDPC coded bits;

an S/P (Serial to Parallel) mapping functional block that divides the variable code rate LDPC codeword into a plurality of paths such that each path of the plurality of paths outputs selected LDPC coded bits of the plurality of LDPC coded bits;

wherein LDPC coded bits that are output from the plurality of paths are grouped together to form a plurality of LDPC coded symbols;

a plurality of modulation encoders operating cooperatively such that each modulation encoder of the plurality of modulation encoders selectively receives certain LDPC coded symbols of the plurality of LDPC coded symbols according to a predetermined cycle;

wherein each modulation encoder of the plurality of modulation encoders performs modulation encoding on the LDPC coded symbols of the plurality of LDPC coded symbols that it receives thereby generating corresponding pluralities of LDPC coded modulation symbols; and

wherein LDPC coded modulation symbols are selected from the corresponding pluralities of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable code rate and modulation signal.

14. The encoder of claim 13, wherein:

the S/P mapping functional block divides the variable code rate LDPC codeword into 3 paths;

a second n bits of the plurality of LDPC coded bits of the variable code rate LDPC codeword are provided to a first path of the 3 paths;

a last n bits of the plurality of LDPC coded bits of the variable code rate LDPC codeword are provided to a second path of the 3 paths; and

a first n bits of the plurality of LDPC coded bits of the variable code rate LDPC codeword are provided to a third path of the 3 paths.

15. The encoder of claim 13, wherein:

the S/P mapping functional block divides the variable code rate LDPC codeword into 3 paths;

a first bit is selected from a first path of the 3 paths;

a second bit is selected from a second path of the 3 paths;

a third bit is selected from a third path of the 3 paths; and

the first bit, the second bit, and the third bit form are grouped together to form a 3 bit LDPC coded symbol.

16. The encoder of claim 13, wherein:

the plurality of modulation encoders includes a first modulation encoder and a second modulation encoder;

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

the first modulation encoder receives all of the LDPC coded symbols of the first plurality of LDPC coded symbols and odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols; and

the second modulation encoder receives even numbered LDPC coded symbols of the second plurality of LDPC coded symbols.

17. The encoder of claim 13, wherein:

the plurality of modulation encoders includes a first modulation encoder, a second modulation encoder, and a third modulation encoder;

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

the first modulation encoder receives all of the LDPC coded symbols of the first plurality of LDPC coded symbols;

the second modulation encoder receives even numbered LDPC coded symbols of the second plurality of LDPC coded symbols; and

the third modulation encoder receives odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols.

18. The encoder of claim 13, wherein:

the plurality of modulation encoders includes a first 8 PSK (8 Phase Shift Key) modulation encoder and a second 8 PSK modulation encoder;

the first 8 PSK modulation encoder performs modulation encoding using a first modulation on the LDPC coded symbols that it receives thereby generating a first corresponding plurality of LDPC coded modulation symbols;

the second 8 PSK modulation encoder performs modulation encoding using a second modulation on the LDPC coded symbols that it receives thereby generating a second corresponding plurality of LDPC coded modulation symbols; and

LDPC coded modulation symbols are selected from the first corresponding plurality of LDPC coded modulation symbols and the second corresponding plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

19. The encoder of claim 13, wherein:

the plurality of modulation encoders includes a first 8 PSK (8 Phase Shift Key) modulation encoder, a second 8 PSK modulation encoder, and a third 8 PSK modulation encoder;

the first 8 PSK modulation encoder performs modulation encoding using a first modulation on the LDPC coded symbols that it receives thereby generating a first corresponding plurality of LDPC coded modulation symbols;

the second 8 PSK modulation encoder performs modulation encoding using a second modulation on the LDPC coded symbols that it receives thereby generating a second corresponding plurality of LDPC coded modulation symbols;

the third 8 PSK modulation encoder performs modulation encoding using a third modulation on the LDPC coded symbols that it receives thereby generating a third corresponding plurality of LDPC coded modulation symbols; and

LDPC coded modulation symbols are selected from the first corresponding plurality of LDPC coded modulation symbols, the second corresponding plurality of LDPC coded modulation symbols, and the third corresponding plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

20. The encoder of claim 13, wherein:

each modulation encoder of the plurality of modulation encoders performs modulation encoding on the LDPC coded symbols of the plurality of LDPC coded symbols that it receives according to a modulation corresponding to that modulation encoder;

each modulation encoder employs a modulation that is different that the modulations employed by the other modulation encoders when performing modulation encoding that is different that the modulation employed by the other modulation encoders; and

each modulation includes a constellation and a corresponding mapping.

21. The encoder of claim 13, wherein:

the LDPC variable modulation signal includes a plurality of LDPC coded modulation symbols;

a first LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a first modulation that includes a first constellation and a corresponding first mapping; and

a second LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a second modulation that includes a second constellation and a corresponding second mapping.

22. The encoder of claim 21, wherein:

the first constellation and the second constellation are both 8 PSK (8 Phase Shift Key) shaped constellations;

the first modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the corresponding first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to the corresponding second mapping.

23. The encoder of claim 13, wherein:

the LDPC coded bits that are output from the plurality of paths are grouped together to form a plurality of LDPC coded symbols such that a first LDPC coded symbol includes a first number of bits and a second LDPC coded symbol includes a second number of bits.

24. The encoder of claim 13, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

25. An encoder that performs both LDPC (Low Density Parity Check) encoding and modulation encoding on a binary sequence to generate an LDPC coded modulation signal, the encoder comprising:

an LDPC encoder that performs LDPC coding on the binary sequence to generate an LDPC codeword that includes a plurality of LDPC coded bits;

an S/P (Serial to Parallel) mapping functional block that divides the LDPC codeword into 3 paths;

wherein a first path of the 3 paths includes a first plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein a second path of the 3 paths includes a second plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein a third path of the 3 paths includes a third plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein, during successive time periods, the S/P mapping functional block outputs 1 bit from the first plurality of LDPC coded bits, 1 bit from the second plurality of LDPC coded bits, and 1 bit from the third plurality of LDPC coded bits such that the output bits are grouped together to generate 3 bit LDPC coded symbols;

wherein the generated 3 bit LDPC coded symbols cooperatively form a plurality of 3 bit LDPC coded symbols such that each 3 bit LDPC coded symbol corresponds to one of the successive time periods;

a first modulation encoder and a second modulation encoder operating cooperatively such each of the first modulation encoder and the second modulation encoder alternatively receives 3 bit LDPC coded symbols of the plurality of 3 bit LDPC coded symbols that are output from the S/P mapping functional block;

wherein the first modulation encoder performs modulation encoding on the 3 bit LDPC coded symbols that it receives according to a first modulation thereby generating a first plurality of LDPC coded modulation symbols;

wherein the second modulation encoder performs modulation encoding on the 3 bit LDPC coded symbols that it receives according to a second modulation thereby generating a second plurality of LDPC coded modulation symbols; and

wherein LDPC coded modulation symbols are selected from the first plurality of LDPC coded modulation symbols and the second plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

26. The encoder of claim 25, wherein:

the plurality of 3 bit LDPC coded symbols includes a first plurality of 3 bit LDPC coded symbols and a second plurality of 3 bit LDPC coded symbols;

the first modulation encoder receives all of the 3 bit LDPC coded symbols of the first plurality of 3 bit LDPC coded symbols and odd numbered 3 bit LDPC coded symbols of the second plurality of 3 bit LDPC coded symbols; and

the second modulation encoder receives even numbered 3 bit LDPC coded symbols of the second plurality of 3 bit LDPC coded symbols.

27. The encoder of claim 25, wherein:

the LDPC variable modulation signal includes a plurality of LDPC coded modulation symbols;

a first LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to a corresponding first mapping; and

a second LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a second modulation that includes the 8 PSK shaped constellation whose constellation points are mapped according to a corresponding second mapping.

28. The encoder of claim 25, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

29. An encoder that performs both LDPC (Low Density Parity Check) encoding and modulation encoding on a binary sequence to generate an LDPC coded modulation signal, the encoder comprising:

an LDPC encoder that performs LDPC coding on the binary sequence to generate an LDPC codeword that includes a plurality of LDPC coded bits;

an S/P (Serial to Parallel) mapping functional block that divides the LDPC codeword into 3 paths;

wherein a first path of the 3 paths includes a first plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein a second path of the 3 paths includes a second plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein a third path of the 3 paths includes a third plurality of LDPC coded bits selected from the plurality of LDPC coded bits;

wherein, during successive time periods, the S/P mapping functional block outputs 1 bit from the first plurality of LDPC coded bits, 1 bit from the second plurality of LDPC coded bits, and 1 bit from the third plurality of LDPC coded bits such that the output bits are grouped together to generate 3 bit LDPC coded symbols;

wherein the generated 3 bit LDPC coded symbols cooperatively form a plurality of 3 bit LDPC coded symbols such that each 3 bit LDPC coded symbol corresponds to one of the successive time periods;

a first modulation encoder, a second modulation encoder, and a third modulation encoder operating cooperatively such each of the first modulation encoder, the second modulation encoder, and the third modulation encoder successively receives 3 bit LDPC coded symbols of the plurality of 3 bit LDPC coded symbols that are output from the S/P mapping functional block according to a predetermined cycle;

wherein the first modulation encoder performs modulation encoding on the 3 bit LDPC coded symbols that it receives according to a first modulation thereby generating a first plurality of LDPC coded modulation symbols;

wherein the second modulation encoder performs modulation encoding on the 3 bit LDPC coded symbols that it receives according to a second modulation thereby generating a second plurality of LDPC coded modulation symbols;

wherein the third modulation encoder performs modulation encoding on the 3 bit LDPC coded symbols that it receives according to a third modulation thereby generating a third plurality of LDPC coded modulation symbols; and

wherein LDPC coded modulation symbols are selected from the first plurality of LDPC coded modulation symbols, the second plurality of LDPC coded modulation symbols, and the third plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

30. The encoder of claim 29, wherein:

the plurality of 3 bit LDPC coded symbols includes a first plurality of 3 bit LDPC coded symbols and a second plurality of 3 bit LDPC coded symbols;

the first modulation encoder receives all of the 3 bit LDPC coded symbols of the first plurality of 3 bit LDPC coded symbols;

the second modulation encoder receives even numbered 3 bit LDPC coded symbols of the second plurality of 3 bit LDPC coded symbols; and

the third modulation encoder receives odd numbered 3 bit LDPC coded symbols of the second plurality of 3 bit LDPC coded symbols.

31. The encoder of claim 29, wherein:

the LDPC variable modulation signal includes a plurality of LDPC coded modulation symbols;

a first LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to a corresponding first mapping;

a second LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a second modulation that includes the 8 PSK shaped constellation whose constellation points are mapped according to a corresponding second mapping; and

a third LDPC coded modulation symbol of the plurality of LDPC coded modulation symbols is modulation encoded according to a third modulation that includes the 8 PSK shaped constellation whose constellation points are mapped according to a corresponding third mapping.

32. The encoder of claim 29, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.

33. An encoding method performs both LDPC (Low Density Parity Check) encoding and modulation encoding on a binary sequence to generate an LDPC coded modulation signal, the method comprising:

performing LDPC coding on the binary sequence to generate an LDPC codeword that includes a plurality of LDPC coded bits;

dividing the LDPC codeword into a plurality of paths such that each path of the plurality of paths outputs selected LDPC coded bits of the plurality of LDPC coded bits;

grouping the LDPC coded bits that are output from the plurality of paths together to form a plurality of LDPC coded symbols;

selectively performing modulation encoding on the plurality of LDPC coded symbols according to a plurality of modulations such that a first LDPC coded symbol of the plurality of LDPC coded symbols is modulation encoded according to a first modulation to form a first LDPC coded modulation symbol and a second LDPC coded symbol of the plurality of LDPC coded symbols is modulation encoded according to a second modulation to form a second LDPC coded modulation symbol; and

arranging the first LDPC coded modulation symbol and the second LDPC coded modulation symbol to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

34. The method of claim 33, further comprising:

dividing the LDPC codeword into 3 paths;

providing a second n bits of the plurality of LDPC coded bits of the LDPC codeword to a first path of the 3 paths;

providing a last n bits of the plurality of LDPC coded bits of the LDPC codeword to a second path of the 3 paths; and

providing a first n bits of the plurality of LDPC coded bits of the LDPC codeword to a third path of the 3 paths.

35. The method of claim 33, further comprising:

dividing the LDPC codeword into 3 paths;

selecting a first bit from a first path of the 3 paths;

selecting a second bit from a second path of the 3 paths;

selecting a third bit from a third path of the 3 paths; and

grouping the first bit, the second bit, and the third bit form together to form a 3 bit LDPC coded symbol.

36. The method of claim 33, wherein:

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

further comprising:

modulation encoding all of the LDPC coded symbols of the first plurality of LDPC coded symbols and odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols according to the first modulation;

modulation encoding even numbered LDPC coded symbols of the second plurality of LDPC coded symbols according to the second modulation.

37. The method of claim 33, wherein:

the plurality of LDPC coded symbols includes a first plurality of LDPC coded symbols and a second plurality of LDPC coded symbols;

further comprising:

modulation encoding all of the LDPC coded symbols of the first plurality of LDPC coded symbols according to the first modulation;

modulation encoding even numbered LDPC coded symbols of the second plurality of LDPC coded symbols according to the second modulation; and

modulation encoding odd numbered LDPC coded symbols of the second plurality of LDPC coded symbols according to the third modulation.

38. The method of claim 33, wherein:

the plurality of modulation encoders includes a first 8 PSK (8 Phase Shift Key) modulation encoder and a second 8 PSK modulation encoder;

the first 8 PSK modulation encoder performs modulation encoding using a first modulation on the LDPC coded symbols that it receives thereby generating a first corresponding plurality of LDPC coded modulation symbols;

the second 8 PSK modulation encoder performs modulation encoding using a second modulation on the LDPC coded symbols that it receives thereby generating a second corresponding plurality of LDPC coded modulation symbols; and

LDPC coded modulation symbols are selected from the first corresponding plurality of LDPC coded modulation symbols and the second corresponding plurality of LDPC coded modulation symbols to form the LDPC coded modulation signal that is an LDPC variable modulation signal.

39. The method of claim 33, wherein:

the first modulation includes a first constellation and a corresponding first mapping; and

the second modulation includes a second constellation and a corresponding second mapping.

40. The method of claim 33, wherein:

the first modulation includes an 8 PSK (8 Phase Shift Key) shaped constellation whose constellation points are mapped according to a corresponding first mapping; and

the second modulation includes the 8 PSK shaped constellation whose constellation points are mapped according to a corresponding second mapping.

41. The method of claim 33, further comprising:

performing variable code rate LDPC coding on the binary sequence to generate the LDPC codeword such that the LDPC codeword is a variable code rate LDPC codeword;

dividing the variable code rate LDPC codeword into the plurality of paths such that each path of the plurality of paths outputs selected LDPC coded bits of the plurality of LDPC coded bits;

grouping together outputs from the plurality of paths to form a plurality of LDPC coded symbols such that a first LDPC coded symbol includes a first number of bits and a second LDPC coded symbol includes a second number of bits; and

wherein:

the formed LDPC coded modulation signal that is an LDPC variable modulation signal is also an LDPC variable code rate signal.

42. The method of claim 33, wherein:

the method is performed within an encoder;

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, a fiber-optic communication system, a WLAN (Wireless Local Area Network) communication system, and a DSL (Digital Subscriber Line) communication system.